General Description

This document provides the interface descriptions, timing details, and functional specifications for the IP Cores, Inc. BCH Encoder (BCH10-E) and BCH Decoder (BCH10-D) hardware modules. These cores implement a Bose-Chaudhuri-Hocquenghem (BCH) error correction code configured to process a k-bit codeword, providing the capability to correct up to t bit errors per block. On the decoder side, more than t errors will be typically detected with "uncorrectable" cff pin asserted.

The core targets the high-performance very-low-latency error correction ASIC applications with high k (about 500) and small t (3-5) using Bose–Chaudhuri–Hocquenghem codes (BCH codes) that prioritize latency over size. The performance of the BCH10 core is 1 word (k bits) per clock (that is, new codeword is produced or accepted on every clock). The clock rates of 2-3 GHz and more are possible in high-speed semiconductor technology nodes.

The latency of the encoder core is 2 clocks. The decoder latency is 5-7[1] clocks input-to-output data.[2]

Key Features

- High performance, low latency
- Small size (75K gates for k=298, t=4)
- Entirely self-contained (no external RAM required)
- Deliverables include Verilog test bench and test vectors
- Data inputs and outputs have flip-flops attached to the pins

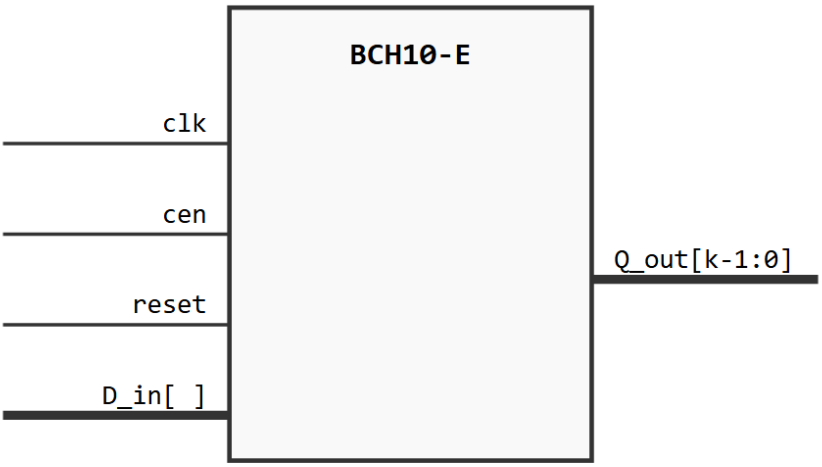
[1] Depends on t

[2] All data inputs and outputs have flip-flops (are registered)

Encoder Core (BCH10-E)

The encoder module takes a unencoded data word input and generates a k-bit encoded codeword. It calculates and appending parity bits to the input data.

Symbol



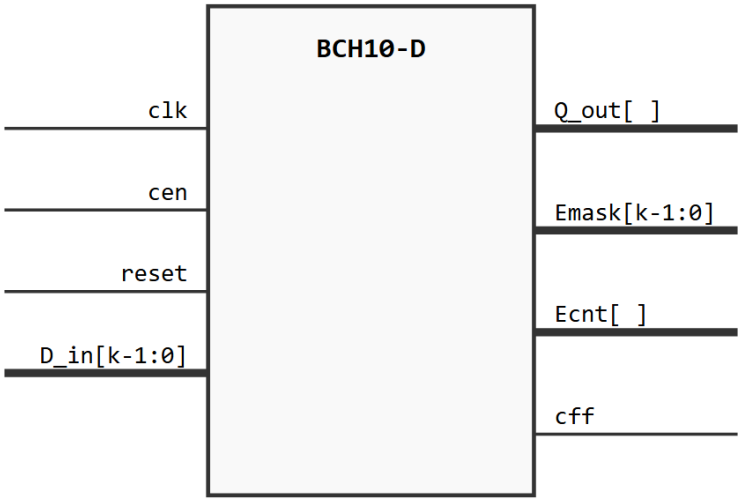
Interface Signals

Signal Name	Direction	Width	Description
clk	Input	1	Clock signal.
cen	Input	1	Clock enable signal. When driven low, it pauses the operation of the core,
reset	Input	1	Active HIGH asynchronous reset signal. Drives internal registers to their default state independent of the clock.
D_in	Input		Data to be encoded
Q_out	Output	k	Codeword

Decoder Core (BCH10-D)

The decoder module ingests the k-bit received codeword, checks for errors, and attempts to correct them. It provides the corrected data along with metadata about the error correction process.

Symbol



Interface Signals

Signal Name	Direction	Width	Description
clk	Input	1	Clock signal.
cen	Input	1	Clock enable signal. When driven low, it pauses the core and pipeline state.
reset	Input	1	Active HIGH asynchronous reset signal.
D_in	Input	k	Received codeword
Q_out	Output		Corrected data payload. Parity bits are stripped.
Emask	Output	k	Errors mask indicating the exact locations of detected errors
Ecnt	Output		Number of errors detected, in the range 0-t. If the number of errors in the input word is greater than t, the core is unable to correct the errors and Q_out and Emask shall not be relied upon
cff	Output	1	Correction Failed Flag: Asserts if there are too many errors. All other outputs in this case are most likely invalid.

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