BCH1-1 Core

Parameterizable compact BCH codec

General Description

The core targets the lower-performance error correction applications using Bose–Chaudhuri–Hocquenghem codes (BCH codes) that prioritize small size over performance. The performance of the BCH1-1 core is approximately 1 bit of the codeword per clock (that is, the m = 9, n=511 word will be handled in slightly more than 511 clocks).[1] For higher performance, larger cores are available in the BCH1 family.

The design is configurable in terms of data size and maximum number of corrected errors. The core, during instantiation, can support one of the Bose-Chaudhuri-Hocquenghem codes BCH(n,k,t)

- m (the exponent in the formula $n = 2^m-1$ for the total number of bits in the codeword) varies between 4 and 9[2] (n is between 15 and 511)
- t (the maximum number of errors that can be corrected) varies between 2 and 16
- for each pair of m and t, the maximum value of k (number of data bits) is determined by (n, t). The "shortened" codes with value of k smaller than the maximum are supported
- the optimal generation polynomial is selected automatically[3].

BCH1 usually comes as two independent encoding and decoding cores, E/D designation indicates the direction. BCH1-1 is very compact, the largest n = 511 t=16 k = 367 decoder occupies just 14K ASIC gates (encoders are much smaller, the companion BCH1-1-511-16E core uses about 2K gates).

During the encoding operation only k data bits need to be provided serially on the D input; *n* bits will be available on the serial output Q; therefore, the encoder will need to backpressure (pause) the input. During the decoding, *n* bits need to be provided on the input, k bits will be available on the output (since the throughput of the decoder is below 1 bit per clock, the decoder might also backpressure the input). The cores request the data on the input bus and indicates the valid data on the output bus via the full set of ready/valid handshaking signals.

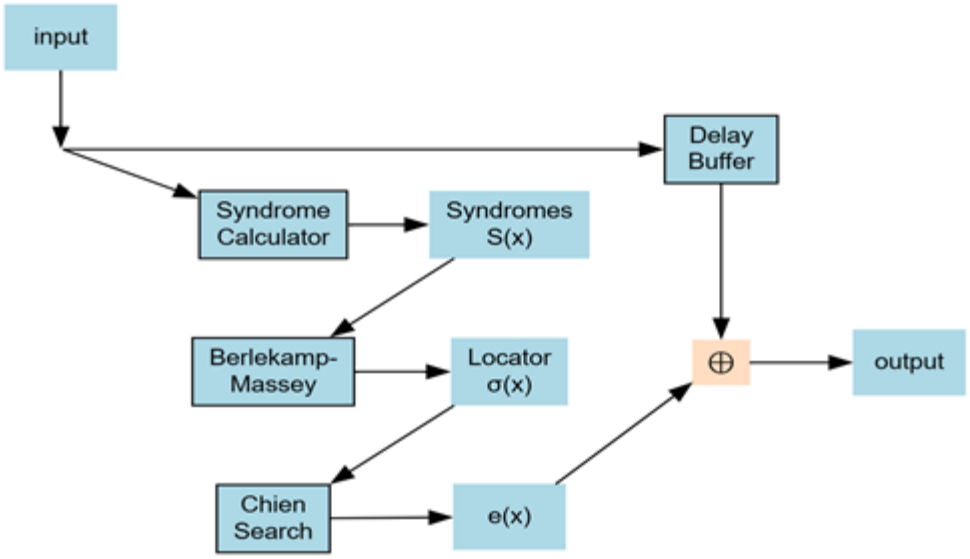
The latency of the encoder core is fixed and very low (few clocks, actual number depends on the configuration). The decoder latency is slightly larger than the codeword size (as the entire codeword needs to be received serially for the decoding).[4]

Architecture

The decoder core utilizes the classical BCH decoder architecture, with separate blocks for syndrome calculator, Berlekamp-Massey algorithm converting syndromes into a locator polynomial, followed by Chien search for roots.

[1] The actual performance slightly varies depending on the parameterization. For example, the largest n=511, t=16 processes approximately 0.8 bits per clock. Performance in terms of data bits (excluding the correction bits will be correspondingly lower).
[2] The architecture has no inherent limitations on n and t, other combinations of n and t can be supported upon request.
[3] Architecture of the core permits parameterization of the polynomial and can be supported upon request.

Output of Chien search contains pulses at the roots of the polynomial (locations of errors) that are XORed with the delayed input data. If there are more than t errors in the input data, and Berlekamp-Massey algorithm detects the condition, the core outputs unmodified data and reports the non-correctable error.



Key Features

Highly parameterizable

Very low area (in the largest, n = 511 t = 16 configuration, the core uses just 17K gates in ASIC)

Entirely self-contained (no external RAM required)

[4] For lower latencies, IP Cores, Inc. offers wider-bus cores

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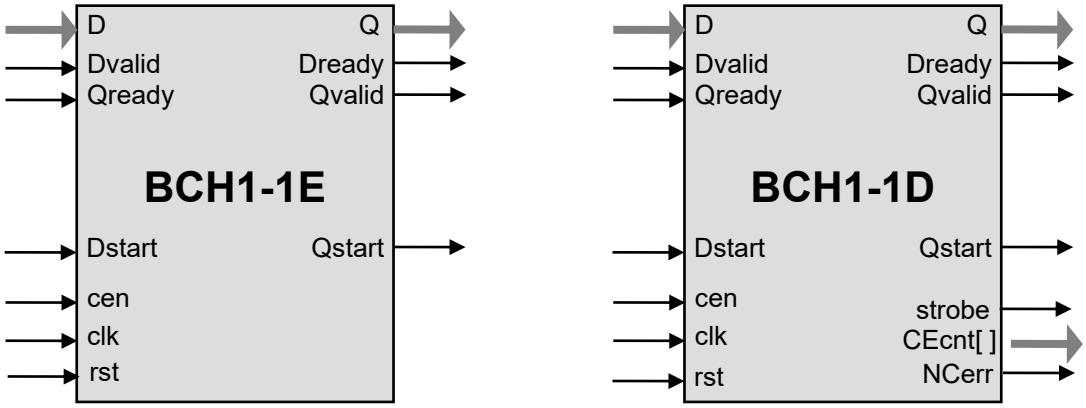
Symbols



Pin Description

Name	Type	Description
clk	Input	Core clock signal
cen	Input	Synchronous enable signal. When LOW the core ignores all its inputs and all its outputs must be ignored.
rst	Input	Synchronous enable signal. When LOW the core is placed into reset.
D	Input	Input Data. For encoder input, the data to be protected by the BCH code. For decoder input, the data to be protected followed by the “error correction” (“parity”) bits.
Q	Output	Output Data. For decoder output, the data to be protected by the BCH code. For encoder output, the data to be protected followed by the “error correction” (“parity”) bits.
Dvalid	Input	HIGH indicated to the core that the valid data is available on the **D** bus
Qvalid	Output	HIGH indicated to the external circuitry that the valid data is available on the **Q** bus
Dready	Output	HIGH indicates to the external circuitry that the core is ready for data on the **D** bus
Qready	Input	HIGH indicated to the core that the external circuitry can accept the data on the **Q** bus
Dstart	Input	A HIGH pulse indicates the start of the input data word (for the -E core) or codeword (for the -D core)
Qstart	Output	A HIGH pulse indicates the start of the output data word (for the -D core) or codeword (for the -E core)
strobe	Output	A HIGH level indicates the validity of the error flags
CEcnt	Output	A number if corrected errors.
NCerr	Output	A non-correctable error flag. HIGH level indicates that non-correctable errors were found, the decoded data shall be ignored.

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