General Description

Implementation of the new WLAN security standard (802.11i) requires the NIST standard AES cipher in CTR and CBC modes (a.k.a. CCM) for encryption and message authentication. The WPA2 AES core is tuned for 802.11i applications and as such requires much smaller gate count than a full implementation. The core contains the base AES core AES1 and is available for immediate licensing.

The design is fully synchronous and available in both source and netlist form.

Key Features

Small size:
8,900 ASIC gates at 802.11a/g OFDM data speeds

Completely self-contained: does not require external memory

Includes encryption, decryption, key expansion and data interface

Support for Counter Mode Encryption (CTR) operation and CCM extensions (Counter Mode with CBC MAC)

Automatic generation of key context from key data

Flow-through design

Test bench provided

Deliverables include test benches

Applications

- WLAN 802.11i
Pin Description

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>Input</td>
<td>Core clock signal</td>
</tr>
<tr>
<td>CEN</td>
<td>Input</td>
<td>Synchronous enable signal. When LOW the core ignores all its inputs and all its outputs must be ignored.</td>
</tr>
<tr>
<td>MODE</td>
<td>Input</td>
<td>Mode. When HIGH, transmit, when LOW receive</td>
</tr>
<tr>
<td>START</td>
<td>Input</td>
<td>HIGH starting input data processing</td>
</tr>
<tr>
<td>READ</td>
<td>Output</td>
<td>Read request for the input data byte</td>
</tr>
<tr>
<td>DATA_VALID</td>
<td>Input</td>
<td>HIGH when valid data byte present on the input</td>
</tr>
<tr>
<td>WRITE</td>
<td>Output</td>
<td>Write to the output interface</td>
</tr>
<tr>
<td>OUT_READY</td>
<td>Input</td>
<td>HIGH when output interface is ready to accept data byte</td>
</tr>
<tr>
<td>D[7:0]</td>
<td>Input</td>
<td>input Data</td>
</tr>
<tr>
<td>Q[7:0]</td>
<td>Output</td>
<td>Output Data</td>
</tr>
<tr>
<td>DONE</td>
<td>Output</td>
<td>Data processing completed</td>
</tr>
</tbody>
</table>

Function Description


The WPA2 implementation fully supports the AES algorithm for 128 bit keys in Counter Mode (CTR) method of encryption with CBC message integrity check as required by the CCM protocol of the 802.11i standard.

The core is designed for flow-through operation, with byte-wide input and output interfaces. CCM key and nonce material precedes the frame in the flow of data. WPA2 supports encrypt and decrypt modes.
Implementation Results

Device Utilization and Performance
Representative area/resources figures are shown below.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Area / Resources</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC 0.18 μ</td>
<td>8900 gates</td>
</tr>
<tr>
<td>Altera FPGA</td>
<td>1362 LUT</td>
</tr>
<tr>
<td>Xilinx FPGA</td>
<td>866 LUT</td>
</tr>
</tbody>
</table>

Export Permits
US Bureau of Industry and Security has assigned the export control classification number 5E002 to the core. The core is eligible for the license exception ENC under section 740.17(A) and (B)(1) of the export administration regulations. See the site of US Department of Commerce [http://www.bxa.doc.gov/Encryption/](http://www.bxa.doc.gov/Encryption/) for details.

Deliverables

**HDL Source Licenses**
- Synthesizable Verilog RTL source code
- Testbench (self-checking)
- Vectors for testbenches
- Expected results
- Simulation script
- Synthesis script
- User Documentation

**Netlist Licenses**
- Post-synthesis EDIF
- Testbench (self-checking)
- Vectors for testbenches
- Expected results
- Place & Route script
- Simulation script

Contact Information
IP Cores, Inc.
3731 Middlefield Rd.
Palo Alto, CA 94303, USA
Phone: +1 (650) 814-0205
E-mail: info@ipcores.com
www.ipcores.com