

### Introduction

The FFT0064 core implements *64 point FFT* in hardware. FFT 64 works on blocks of 64 complex data samples.

Test bench with fixed point Matlab model

Matlab model can be used to tune the bit-width to get the SQNR

Available in ASIC and FPGA technologies

Minimal gate count implementation

Supports flushing and re-starting the FFT operation instantly

### Features

Supports both FFT and IFFT

In built bit reversal algorithm

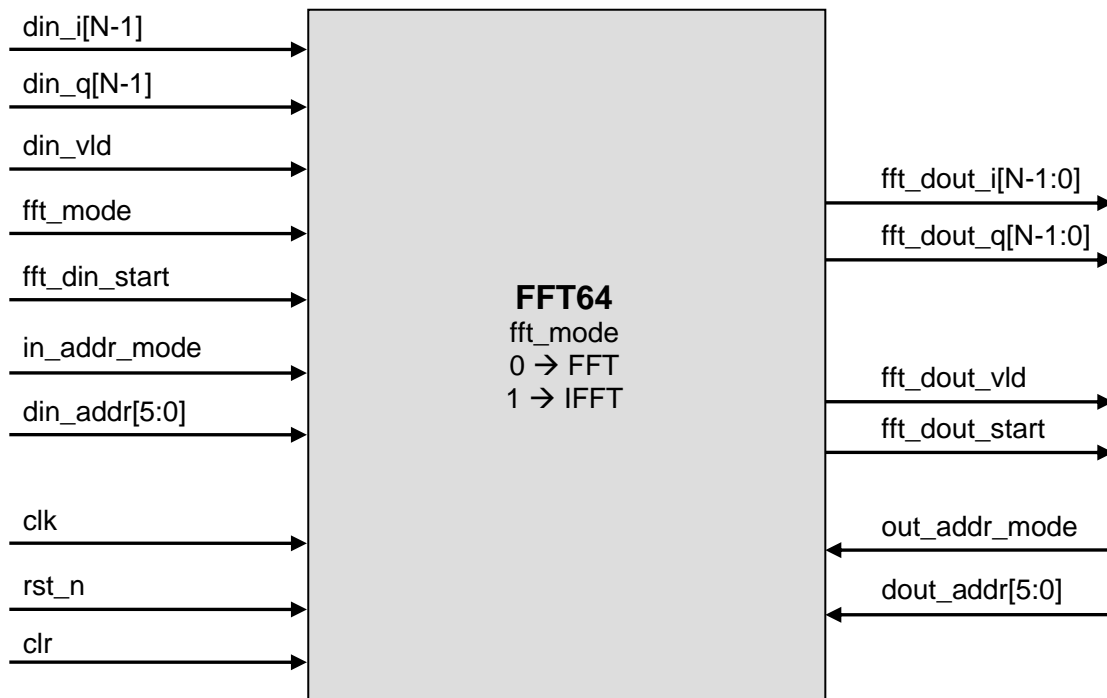
Low Latency

Throughput of 1 sample per clock

Parameterized bit widths and fixed point option.

### Applications

- IEEE802.11 Wi-Fi
- GPS
- Communication system



FFT0064 Block Diagram

## Pin Description

Name	I/O	Width	Description
	1	In	Clock
	1	In	Active low asynchronous reset
CLR	1	In	Active high synchronous reset
FFT_MODE	1	In	0: FFT operation 1: IFFT operation
	N	In	N bit in-phase input data
	N	In	N bit quad-phase input data
	1	In	Input Data Valid
	1	In	Start the FFT computation. This signal should be asserted either on the last input data sample or anytime after sending all input data. Internal FFT engine will start FFT computation when <code>fft_din_start</code> is sampled high on the clock edge. FFT output will be available after fixed latency.
	1	In	Input Address mode. 1'b0 → Use internal addressing to store input data into the internal buffers. 1'b1 → Use external addressing ( <code>din_addr</code> ) to store input data into the internal buffers.
	6	In	Input address when <code>in_addr_mode</code> is set to 1.
	1	In	Output Address mode. 1'b0 → Use internal addressing to read the FFT output data from the internal buffers. 1'b1 → Use external addressing ( <code>dout_addr</code> ) to read the FFT output data from internal buffers.
	6	In	Output address when <code>out_addr_mode</code> is set to 1.
FFT_DOUT_I	N	Out	N bit in-phase output data
FFT_DOUT_Q	N	Out	N bit quad-phase output data
FFT_DOUT_VLD	1	Out	Output Data Valid
FFT_DOUT_START	1	Out	Asserted on the first output point of FFT. This signal is asserted after fixed latency from <code>fft_din_start</code> .

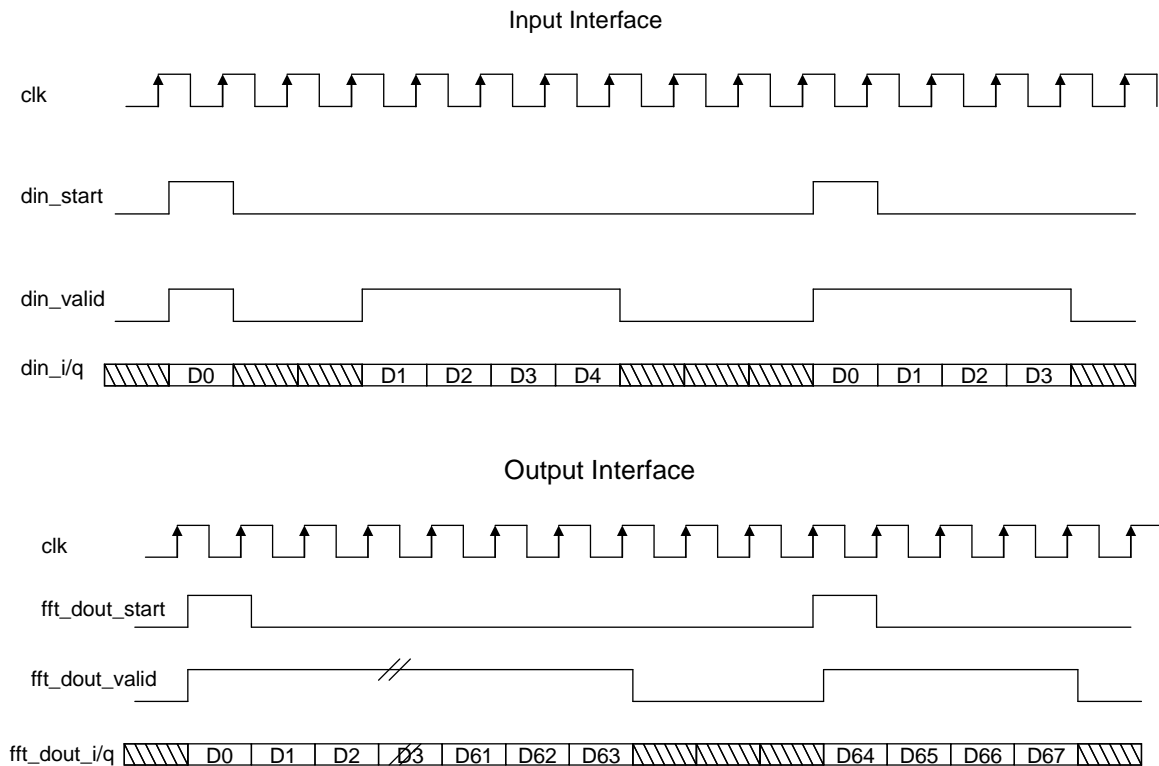
## Function Description

FFT0064 can process 64 pt FFT or 64 pt IFFT based on input mode (fft\_mode). The mode can be switched dynamically. FFT0064 supports two different modes of input data/output data streaming.

- a. Natural order: In natural order the input buffer addressing is controlled internally. On reset the internal address is set to 0 corresponding to the first fft/iff input point.
- b. In external address mode, (in\_addr\_mode == 1), the input data is stored inside internal buffer at the location indicated by din\_addr.

The FFT or IFFT radix operations start when fft\_din\_start pulse is sampled high. The FFT data output will be streamed out after fixed latency. The fft\_dout\_start pulse is asserted on the first output data sample. Similar to input address mode, output address mode can also be controlled internally or externally by providing dout\_addr.

## Interface Timing Diagram



FFT0064 Timing Diagram

### Deliverables

- Synthesizable Verilog RTL source code
- Fixed-point Octave (Matlab compatible) model.
- Simulation scripts
- Self-checking Test environment
  - Test-bench
  - Test-vectors
  - Expected results
- Synthesis scripts
- User Documentation

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