General Description

Implementation of the new WPAN security standard (802.15.3) requires the NIST standard AES cipher in CTR and CBC modes (a.k.a. CCM) for encryption and message authentication. The CCM3 AES core is tuned for 802.15.3 applications and as such requires much smaller gate count than a full implementation. The core contains the base AES core AES1 and is available for immediate licensing.

The design is fully synchronous and available in both source and netlist form.

Key Features

- Small size: From 9,500 ASIC gates at 802.15.3 data speeds
- Completely self-contained: does not require external memory
- Includes encryption, decryption, key expansion and data interface
- Support for Counter Mode Encryption (CTR) operation and CCM extensions (Counter Mode with CBC MAC)
- Automatic generation of key context from key data
- Flow-through design
- Test bench provided

Applications

- IEEE 802.15.3
Pin Description

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>Input</td>
<td>Core clock signal</td>
</tr>
<tr>
<td>CEN</td>
<td>Input</td>
<td>Synchronous enable signal. When LOW the core ignores all its inputs and all its outputs must be ignored.</td>
</tr>
<tr>
<td>MODE</td>
<td>Input</td>
<td>Mode. When HIGH, transmit, when LOW receive</td>
</tr>
<tr>
<td>START</td>
<td>Input</td>
<td>HIGH starting input data processing</td>
</tr>
<tr>
<td>READ</td>
<td>Output</td>
<td>Read request for the input data byte</td>
</tr>
<tr>
<td>DATA_VALID</td>
<td>Input</td>
<td>HIGH when valid data byte present on the input</td>
</tr>
<tr>
<td>WRITE</td>
<td>Output</td>
<td>Write to the output interface</td>
</tr>
<tr>
<td>OUT_READY</td>
<td>Input</td>
<td>HIGH when output interface is ready to accept data byte</td>
</tr>
<tr>
<td>D[i]</td>
<td>Input</td>
<td>input Data</td>
</tr>
<tr>
<td>Q[i]</td>
<td>Output</td>
<td>Output Data</td>
</tr>
<tr>
<td>DONE</td>
<td>Output</td>
<td>Data processing completed</td>
</tr>
</tbody>
</table>

Function Description


The CCM3 implementation fully supports the AES algorithm for 128 bit keys in Counter Mode (CTR) method of encryption with CBC message integrity check as required by the CCM protocol of the 802.15.3 standard.

The core is designed for flow-through operation, with byte-wide input and output interfaces. CCM key and nonce material precedes the frame in the flow of data. CCM3 supports encrypt and decrypt modes.
Implementation Results

Device Utilization and Performance
Representative area/resources figures are shown below.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Area / Resources</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC 0.18 u</td>
<td>9500 gates</td>
</tr>
</tbody>
</table>

Export Permits

US Bureau of Industry and Security has assigned the export control classification number 5E002 to the core. The core is eligible for the license exception ENC under section 740.17(A) and (B)(1) of the export administration regulations. See the site of US Department of Commerce [http://www.bxa.doc.gov/Encryption/] for details.

Deliverables

**HDL Source Licenses**
- Synthesizable Verilog RTL source code
- Testbench (self-checking)
- Vectors for testbenches
- Expected results
- Simulation script
- Synthesis script
- User Documentation

**Netlist Licenses**
- Post-synthesis EDIF
- Testbench (self-checking)
- Vectors for testbenches
- Expected results
- Place & Route script
- Simulation script

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